What is claimed is:

1. A non-volatile memory device comprising:

a memory cell array including a plurality of memory cells arranged in a row direction and a column direction; and

a power supply circuit supplying a voltage to the memory cells, wherein:

each of the memory cells has a source region, a drain region, a channel region disposed between the source region and the drain region, a word gate and a select gate disposed over the channel region with an insulator interposed, and a non-volatile memory element formed between the word gate and the channel region; and

the power supply circuit has a precharge voltage supply section which supplies a precharge voltage to be applied to all the word gates in the memory cell array during standby mode.

2. The non-volatile memory device as defined in claim 1,

wherein all voltages applied to the word gates in the memory cell array are set to the precharge voltage when data is read from a selected memory cell among the memory cells.

3. The non-volatile memory device as defined in claim 2, wherein:

the memory cell array further includes a plurality of word lines extending in the row direction, the word gates of the memory cells in each of the rows being connected in common to one of the word lines; and

all voltages of the word lines are set to the precharge voltage during the standby mode and in the reading.

4. The non-volatile memory device as defined in claim 3, wherein:

the memory cell array further includes a plurality of select lines extending in the row direction, the select gates of the memory cells in each of the rows being connected in common to one of the select lines; and

row selection is performed in the reading by applying a selected voltage to a selected select gate which is connected to a selected memory cell selected in the reading, and by applying a non-selected voltage to a non-selected select gate.

5. The non-volatile memory device as defined in claim 1,

wherein voltages applied to all the word gates connected to a non-selected word line among the word lines are set to the precharge voltage when a memory cell selected from the memory cells is programmed by applying a selected word voltage to a selected word line connected to the selected memory cell.

6. The non-volatile memory device as defined in claim 1, wherein:

the memory cell array is divided into a plurality of blocks for erasing; and

at least one of the blocks is selected for erasing when the precharge voltage is supplied to the word line in a non-selected block.

7. The non-volatile memory device as defined in claim 1,

wherein the precharge voltage supply section supplies a power voltage as the precharge voltage.

8. The non-volatile memory device as defined in claim 1, wherein:

each of the memory cells includes a first region adjacent to the source region and a second region adjacent to the drain region, both the first and second regions being within the channel region; and

the select gate is disposed over the first region, and the non-volatile memory

element is disposed between the word gate and the second region.

9. The non-volatile memory device as defined in claim 1, wherein:

each of the memory cells includes a first region adjacent to the source region and a second region adjacent to the drain region, both the first and second regions being within the channel region; and

the non-volatile memory element is disposed between the word gate and the first region, and the select gate is disposed over the second region.

10. The non-volatile memory device as defined in claim 1,

wherein the non-volatile memory element is formed of an ONO film which includes two oxide films (O), and a nitride film (N) disposed between the two oxide films (O).

11. The non-volatile memory device as defined in claim 1,

wherein the non-volatile memory element is disposed between the select gate and the word gate.

12. The non-volatile memory device as defined in claim 10,

wherein the insulator is formed of one of the two oxide films.